香港中文大學
The Chinese University of Hong Kong

CENG3430 Rapid Prototyping of Digital Systems

Lecture 00: Course Information

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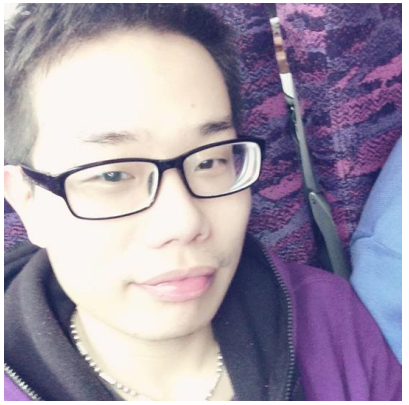
CENG3430 Course Information

- **CENG3430 Rapid Prototyping of Digital Systems**
- **Course Time and Place**
  - **Lecture** (*2)
    - MON 16:30~18:15 (@ ERB 404)
  - **Lab** (*2)
    - TUE 16:30~18:15 (@ SHB 102)

    Note: You‘re required to attend BOTH lab sessions.
- **Course Website**
  - http://www.cse.cuhk.edu.hk/~mcyang/ceng3430/2020S/ceng3430.html
  - https://blackboard.cuhk.edu.hk/

Course Instructor & Teaching Assistants

- **Course Instructor**
  - Prof. Ming-Chang YANG (楊明昌)
    - Office: SHB 906 (3943-8405)
    - Office Hours: MON 14:30~16:30
    - Email: mcyang@cse.cuhk.edu.hk
- **Teaching Assistants**
  - Tinghuan CHEN (陳庭歡)
    - Office: SHB 905
    - Office Hours: TUE 10:00~13:00
    - Email: thchen@cse.cuhk.edu.hk
  - Guangliang YAO (姚廣亮)
    - Office: SHB 1026
    - Office Hours: MON 12:30~14:30
    - Email: glyao@cse.cuhk.edu.hk



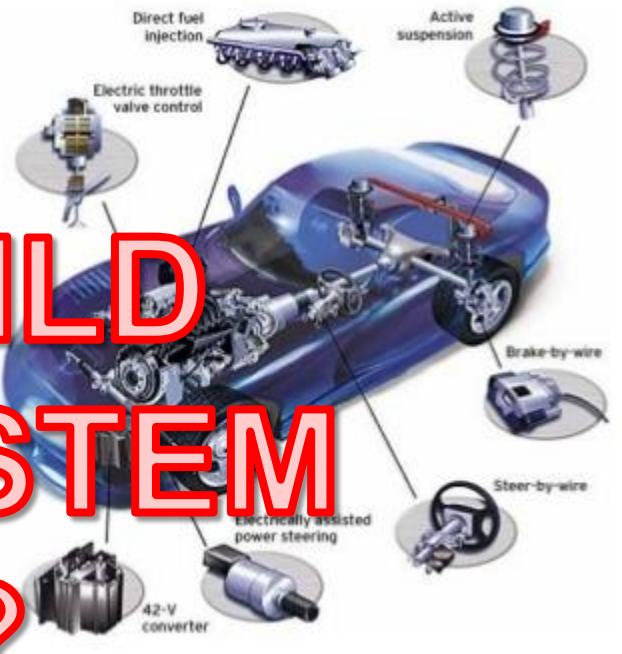
Course Assessment

- Grading *(subject to changes)*
  - Class Exercises 10%
  - Laboratory Exercises 25%
  - Final Project 40%
  - Final Exam 25%
  - *Bonus* *5%* (How to get? Q&A, Best Project)

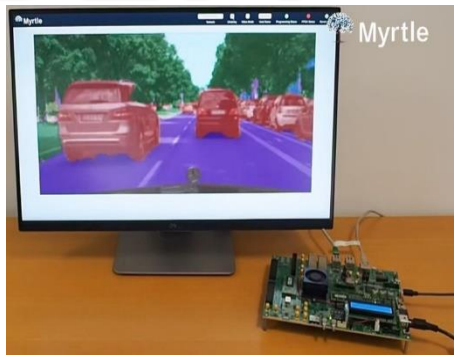
- Notes
  - Lab. exercises and final project: two students in a group.
  - Late submission per day is subject to 10% of penalty.
  - A student must attend at least 80% of lectures in order to gain all class attendance/exercise credits.

We Are Surrounded by Digital Systems

- Mass Products
  - Media players
  - Mobile phones
- Novel Products
  - Wearable devices
  - Robots
- Research
  - Real time edge detection
  - Deep learning acceleration



HOW TO BUILD A DIGITAL SYSTEM RAPIDLY?



Common Design Flow of Digital System

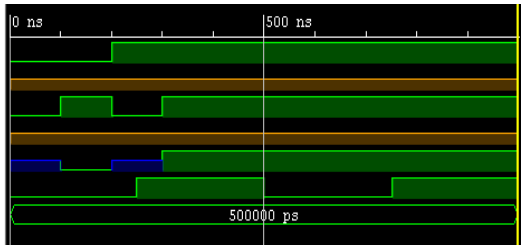
Idea Generation

Drafting on Paper

Designing Chip (VHDL)

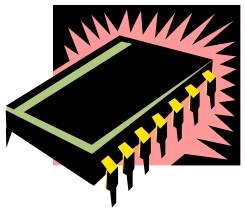
Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
3         c: out std_logic);
4 end and2
5 architecture arch of and2
6 begin
7    c <= a and b;
8 end and2_arch
```



Testing (FPGA)

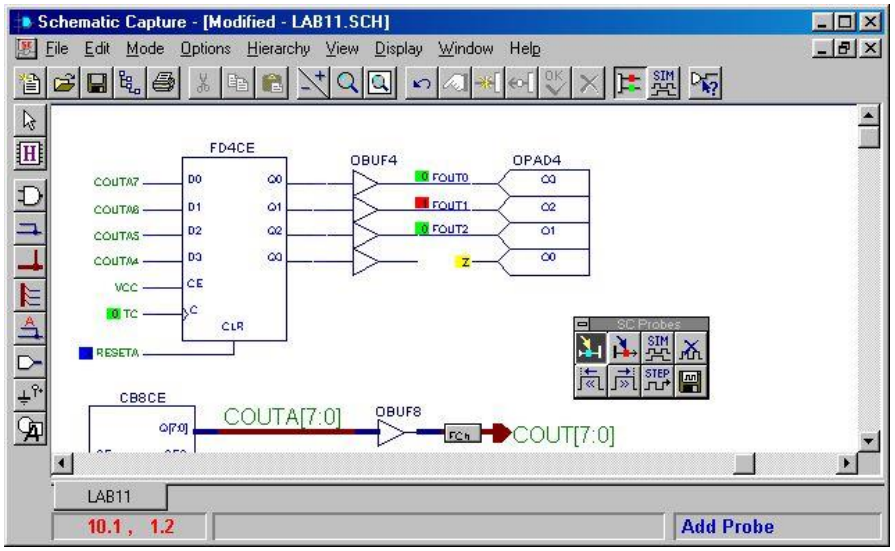
Manufacturing
Production Line Design



Quality Control

Methods for Digital System Design

- **Schematic**
  - Complicated
  - Suitable for top level design to merge modules
    - Like data flow block diagram



- **Language**
  - VHDL (**V**ery-High-Speed-Integrated-Circuits **H**ardware **D**escription **L**anguage)
    - Each module in the schematic can be implemented by VHDL
  - Verilog

Ex: VHDL AND-Gate Program

```
1 entity and2 is
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3         c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
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8 end and2_arch
```

What You Will Learn

- **Software**: Hardware Description Languages (HDL)

Ex: VHDL AND-Gate Program

```
1 entity and2 is
2 port (a,b: in std_logic;
3         c: out std_logic);
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5 architecture and2_arch of and2
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```
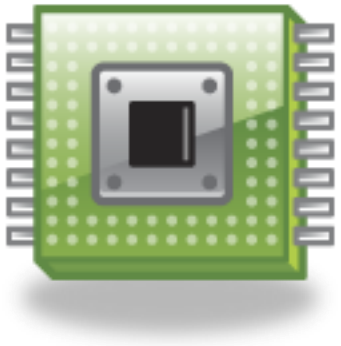
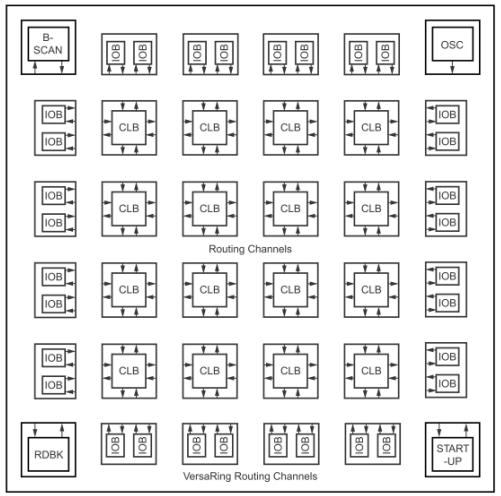

Write HDL code, then it will generate the hardware chip automatically



- **Hardware**: Field Programmable Gate Array (FPGA)
  - The hardware can be reprogrammable.
  - Designs can be changed easily.
  - No additional hardware manufacturing cost is needed.



Our Focus: Prototyping

Idea Generation

Drafting on Paper

Designing Chip (VHDL)

Ex: VHDL AND-Gate Program

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1 entity and2 is
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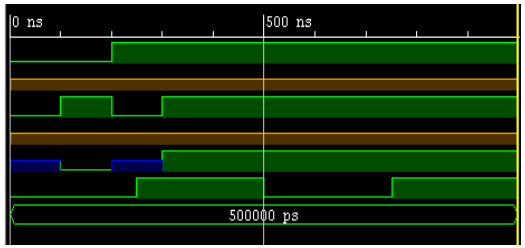
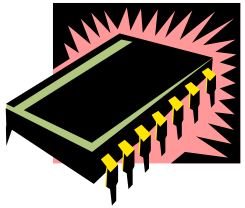


Testing (FPGA)

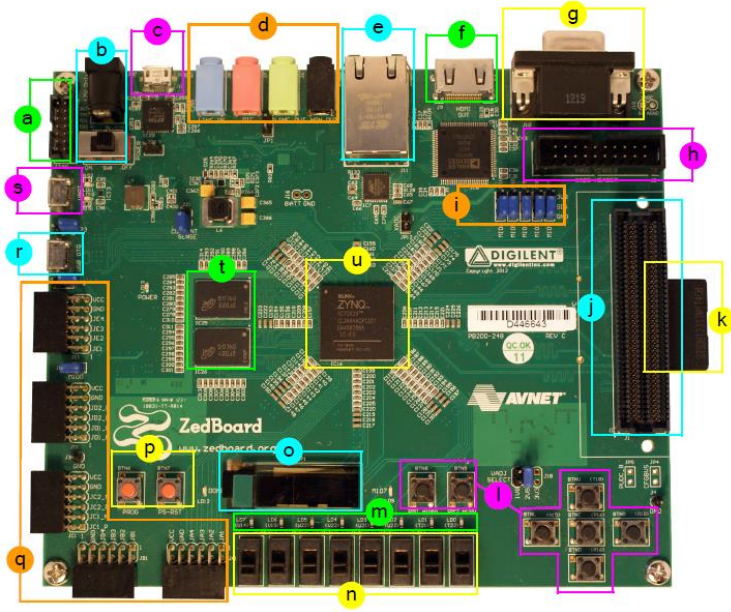
Manufacturing
Production Line Design



Quality Control

What We Will Use in Our Lab

- **Software**: VHDL (*mainly*)
  - **V**ery-High-Speed-Integrated-Circuits (VHSIC) **H**ardware **D**escription **L**anguage
- **Hardware**: Zynq ZedBoard
  - Dual-core ARM Cortex-A9, with
  - Traditional Field Programmable Gate Array (FPGA)



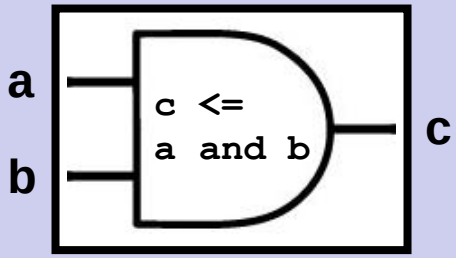
a Xilinx JTAG connector
b Power input and switch
c USB-JTAG (programming)
d Audio ports
e Ethernet port
f HDMI port (output)
g VGA port
h XADC header port
i Configuration jumpers
j FMC connector
k SD card (underside)
l User push buttons
m LEDs
n Switches
o OLED display
p Prog & reset push buttons
q 5 x Pmod connector ports
r USB-OTG peripheral port
s USB-UART port
t DDR3 memory
u Zynq device (+ heatsink)

Software: VHDL

- **An Example: AND-Gate in VHDL**

Entity Declaration: Define I/Os

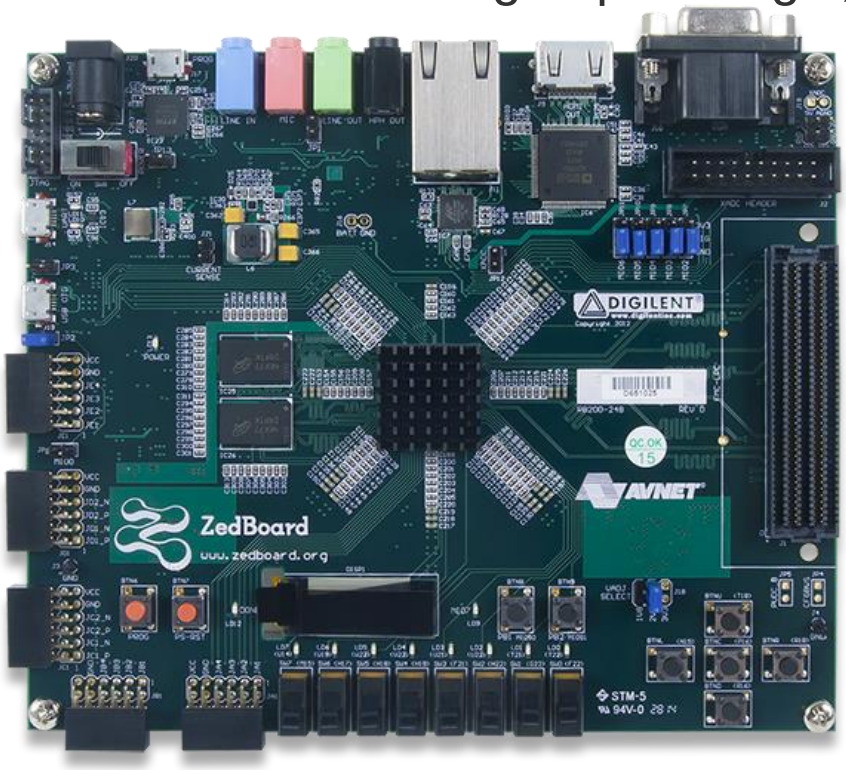
```
1 entity and2 is
2 port (a,b: in std_logic;
3           c: out std_logic);
4 end and2
5 architecture and2_arch of and2
6 begin
7     c <= a and b;
8 end and2_arch
```

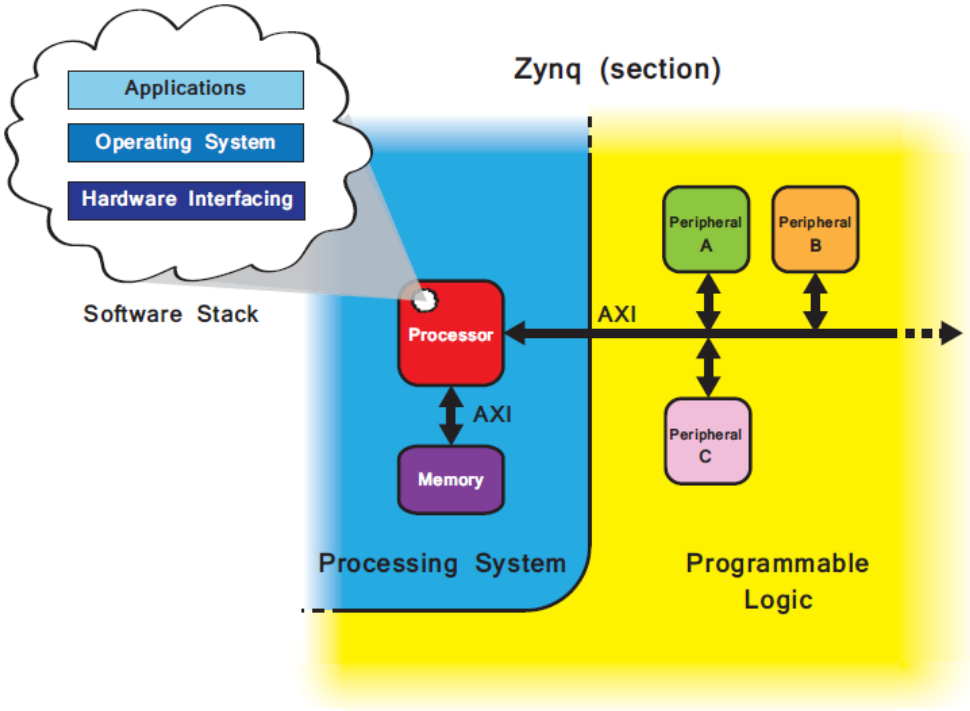


Architecture Body: Define functions

Hardware: Zynq ZedBoard

- Zynq ZedBoard combines
  - Processing System (PS): Dual-core ARM Cortex-A9 CPU
    - Supports software routines and/or operating systems
  - Programmable Logical (PL): Equivalent to trad. FPGA
    - Ideal for high-speed logic, arithmetic and data flow subsystems





Course Schedule

W	Date	Lecture	Lab
1	Jan 6, 7	Lec00: Course Information	No lab
2	Jan 13, 14	Lec01: Introduction to VHDL	Lab01: Vivado & Software Simulation
3	Jan 20, 21	Lec02: Introduction to ZedBoard	Lab02: First Program on ZedBoard
4	Jan 27, 28	Lunar New Year Vacation (No class)	No lab
5	Feb 3, 4	Lec03: Architectural Styles of VHDL	Lab03: 4-to-1 Multiplexer
6	Feb 10, 11	Lec04: Building Blocks of a Processor	Lab04: Serial-in-parallel-out Shift Register
7	Feb 17, 18	Lec05: Use of Clock and Pmod	Lab05: Driving Seven Segment Display
8	Feb 10, 11	Lec06: Finite State Machine	Lab06: Driving VGA Display
9	Feb 17, 18	Lec07: IP Block Design	Lab07-1: Software Stopwatch
10	Feb 10, 11	Lec08: Embedded Operating System	Lab07-2: DDR Memory Block Design
11	Feb 17, 18	Final Project Proposal	Lab08: Linux GPIO + LED
12	Mar 23, 24	Lec09: High Level Synthesis	Lab09: High Level Synthesis Exercise
13	Mar 30, 31	Reading Week (No class)	No lab
14	Apr 6, 7	Lec10: Introduction to Verilog	Lab10: Verilog Exercise
15	Apr 13, 14	Public holiday – Easter (No class)	Final Project Demonstration

Final Project Examples (2017-2018)

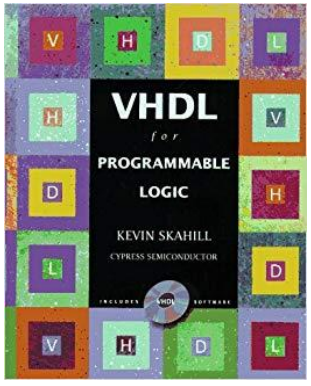
- Piano: https://youtu.be/_VH3fUazEEI?t=87
- Music Player: https://youtu.be/dEdnp1Tni9c?t=27
- Bullhorn: https://youtu.be/dtQ88yL0FUM?t=26
- Wash Machine: https://youtu.be/z7C8dXn9EQ0?t=10
- Thermometer: https://youtu.be/i0swDnATRt4?t=41
- Space Invader: https://youtu.be/2wEG-U8DNak?t=72
- Tetris: https://youtu.be/JyEU1YbYMrc?t=11
- Snake: https://youtu.be/dFdr0KqXw7Q?t=66
- Car: https://youtu.be/FDbSyYKHYes?t=28
- Sonar: https://youtu.be/DiLjDbkbejs?t=180

Final Project Examples (2018-19)

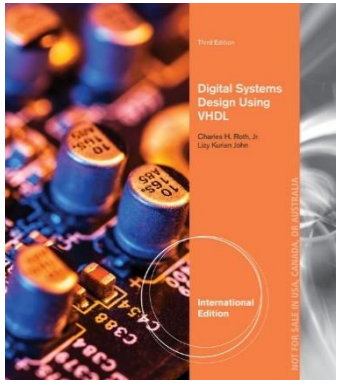
1. Piano and Music Player
2. Color Recognition
3. RGB Meter
4. Lie Detector
5. Snake Battle
6. Space War
7. The Dodge Game
8. Space Impact
9. Get It at Once
10. Elevator
11. Super Pads
12. Tetris
13. Morse Code Interpreter
14. The Flash
15. Multifunctional Display
16. Rolling Down!

References

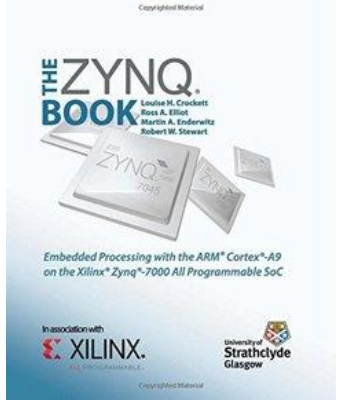
- **VHDL for Programmable Logic**
  - Kevin Skahill
  - Addison-Wesley



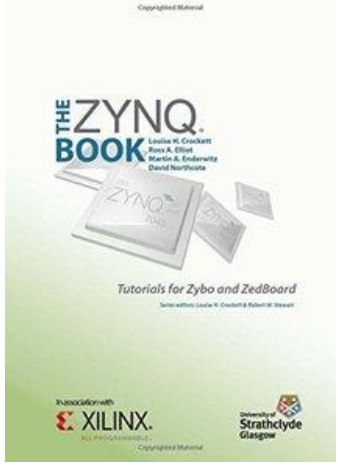
- **Digital Systems Design Using VHDL**
  - Charles H. Roth Jr., Lizy Kurian John
  - Cengage Learning



- **The Zynq Book**: Embedded Processing with the Arm Cortex-A9 on the Xilinx Zynq-7000 All Programmable Soc
  - Louise H Crockett, Ross A Elliot, Martin A Enderwitz, Robert W Stewart
  - Strathclyde Academic Media



- **The Zynq Book**: Tutorials for Zybo and ZedBoard
  - Louise H Crockett, Ross A Elliot, Martin A Enderwitz
  - Strathclyde Academic Media



Important Notes

- Visit our course website regularly!

- Plagiarism will **NOT** be tolerated!
  - Don't copy!
  - Don't let other(s) copy!
  - Can discuss but write up the solutions by yourself!

- Honesty in Academic Work:
  - http://www.cuhk.edu.hk/policy/academichonesty/

The best way to learn is through practice!